www.kaztek.com

WS_CCESSH

System Development with CCES and the ADI SHARC Processor

Course Name:	System Development with CrossCore Embedded Studio (CCES) and the ADI SHARC Processor
Course Code:	WS_CCESSH
Course Description:	This is a practical and interactive course that is designed to systematically teach how to use the SHARC processor to its fullest potential. Emphasis is placed on understanding the steps required to create an efficient SHARC CPU based system in the way that ADI had intended the processor to be used. Several hands on exercises provide an opportunity for the instructor to work one on one with the attendee. Throughout the workshop, attendees are encouraged to ask questions. The CrossCore Embedded Studio (CCES) IDE is covered in detail, including topics on navigating through the IDE, projects and project configuration, the build process, and debug features. Tools based optimizations including compiler and linker optimization are covered. An understanding of the SHARC architecture will enable getting the best performance out of the processor. Architecture topics covered include the core elements of the SHARC, which includes the Computational Units, the Data Address Generators, and the Program Sequencer. The core section is common to all members of the SHARC family. Memory configuration (both internal and external) is discussed next. Advanced instructions and SIMD operation are presented with a follow on lab on code optimization. The I/O peripherals, which include the DAI and DPI, are discussed in detail along with DMA operation between these peripherals and internal memory. A section on booting covers what happens during the boot process, creating boot image files, and discussing how to get them into the target system. Hardware development tools, such as evaluation boards and ICE's are also covered, including setting up hardware debug sessions and other hardware debug topics. An introduction into Micrium's uC/OS is also covered in the workshop. Throughout the course, a number of hands on exercises will take the attendee through the various aspects of the software development process. Topics covered through exercises include setting up and building projects, C and Assembly language programming, various optimizations, code debugging (simulation and hardware), and software module support (eg System Services and Device Drivers).
Goals and Objectives:	The main course objective is to understand the SHARC architecture (with a focus on the ADSP-2136x/37x/4xx Sharc Processor Family members) sufficiently to enable DSP system designers to resolve hardware/software issues with their applications. Additional goals include gaining a thorough understanding of SHARC code development (using both assembly and 'C') using the CCES tool chain.
Pre-requisites:	Previous embedded microprocessor experience would be an asset (hardware and/or software).
Target Audience:	System Designers needing to make informed decisions on design tradeoffs, Hardware Designers needing to develop external interfaces and low level code, and Code Developers needing to know how to get the highest performance from their algorithms
Duration:	3.5 days