



**System Development and Programming
with the ADSP-BF533/7 Families**

Course Name:	System Development and Programming with the ADSP-BF533/7 Families
Course Code:	WS_BF533/7
Course Description:	<p>This is a practical and interactive course that is designed to systematically teach how to use the Blackfin processor to its fullest potential. Emphasis is placed on understanding the steps required to create an efficient Blackfin CPU based system in the way that ADI had intended the processor to be used. Several hands on exercises provide an opportunity for the instructor to work one on one with the attendee. Throughout the workshop, attendees are encouraged to ask questions.</p> <p>The VisualDSP++ IDDE is covered in detail, including topics on projects and project configuration, the build process, and debug features. Tools based optimizations including compiler and linker optimization are covered. The salient features of System Services and Device Drivers are first introduced. Later sections on specific peripherals or system features will connect back to the related Services or Driver API. An understanding of the Blackfin architecture will enable getting the best performance out of the processor. Architecture topics covered include loop/branch optimization and interrupt handling, L1 Memory configuration (ie L1 SRAM and Cache), specialized instructions including the quad 8-bit Video ALU operations, and DMA operation between peripherals and memory, as well as from memory to memory. The usage and capabilities of the various I/O and timer peripherals are discussed in detail. A section on booting covers what happens during the boot process, creating boot image files, and discussing how to get them into the target system. Hardware considerations such as operation of the power management and reset are also discussed. Hardware development tools, such as evaluation boards and ICE's are also covered, including setting up hardware debug sessions and other hardware debug topics. An introduction into VDK (Visual DSP Kernel) is also covered in the workshop.</p> <p>Throughout the course, a number of hands on exercises will take the attendee through the various aspects of the software development process. Topics covered through exercises include setting up and building projects, C language programming (eg using intrinsics, exploring different data types), various optimizations (eg compiler, linker, mixed C/assembly), code debugging (eg profiling, plotting, pipeline analysis), simulation (eg DMA, interrupts, stream I/O), and 'C' programming support (eg System Services and Device Drivers). One set of exercises will focus on bringing the various elements together (eg peripheral setup, DMA, interrupts, etc) in the setup of a typical application framework, initially in straight C and later using the System Services and Device Drives programming model.</p>
Goals and Objectives:	The main course objective is to instill to the attendee a high level of confidence to create an efficient Blackfin® Processor based system. By being exposed to the various capabilities and features of the Blackfin processor and VDSP tool chain, the attendee will be better armed to tackle any issues that arise in their specific system implementations.
Pre-requisites:	Previous embedded microprocessor experience would be an asset (hardware and/or software). It is also highly recommended to take in the Blackfin Online Learning and Development (BOLD) Video Tutorial entitled "Blackfin® Core Architecture"
Target Audience:	System Designers needing to make informed decisions on design tradeoffs, Hardware Designers needing to develop external interfaces and low level code, and Code Developers needing to know how to get the highest performance from their algorithms
Duration:	3.5 days



- 1 Introduction**
 - 1.1 Goal of Workshop**
 - 1.2 Course Overview**
 - 1.3 Course Handouts**
 - 1.4 Characteristics of a Good Embedded Processor**
 - 1.5 Characteristics of a Good DSP**
 - 1.6 ADSP-BF533 Architecture Overview**
 - 1.7 ADSP-BF537 Architecture Overview**
 - 1.8 Clock Domains**

- 2 Introduction to Software Tools**
 - 2.1 VisualDSP++ Overview**
 - 2.1.1 Software Development Process**
 - 2.2 IDDE and Projects**
 - 2.2.1 Creating projects and the Project Wizard**
 - 2.2.2 Project Options and Build Configurations**
 - 2.3 Invoking the Tools**
 - 2.4 Debug Sessions**
 - 2.5 Debugger Features**
 - 2.5.1 Debug control**
 - 2.5.2 Debug windows**
 - 2.5.3 Profiling**
 - 2.6 Help**
 - 2.7 Exercise – “Hello World”**
 - 2.8 System Services and Device Drivers**
 - 2.8.1 What are they?**



2.9 Services Overview

- 2.9.1 Interrupt Manager**
- 2.9.2 EBIU Service**
- 2.9.3 Dynamic Power Management Service**
- 2.9.4 Port Control Service**
- 2.9.5 Deferred Callback Manager**
- 2.9.6 DMA Manager**
- 2.9.7 Programmable Flag Service**
- 2.9.8 Timer Service**
- 2.9.9 RTC (Real Time Clock) Service**
- 2.9.10 File System Service**
- 2.9.11 Semaphore Service**

2.10 Drivers Overview

- 2.10.1 Device Driver API**
- 2.10.2 Relationship to Services**
- 2.10.3 Data Buffers**
- 2.10.4 Data Flow Types**
- 2.10.5 Off Chip Drivers**

2.11 Finding Additional Information

3 Blackfin Core Review

3.1 Fixed Point Numbering Formats

- 3.1.1 Built-in Support for Fractional Data Types**

3.2 Registers

- 3.2.1 Core Registers**
- 3.2.2 Memory Mapped Registers**
- 3.2.3 Register File**

3.3 Arithmetic Units

- 3.3.1 Features**
- 3.3.2 Arithmetic Logic Unit (ALU)**
- 3.3.3 Multiplier/ Accumulator (MAC)**
- 3.3.4 Shifter**
- 3.3.5 Example Instructions**



3.4 Fetching Data

3.4.1 Data Address Generators (DAG) Features

3.4.2 Data Move Examples

3.4.3 Address Pointer Manipulation

3.4.4 Stack Operations

3.4.5 DSP Addressing

3.4.5.1 Circular Buffering

3.4.5.2 Bit Reversal

3.5 Simulator Exercise

4 Memory

4.1 Features

4.1.1 Memory Levels

4.1.2 Configurable L1 Memory

4.1.3 BF533/7 Memory Variants

4.1.4 Memory Maps

4.2 L1 Memory

4.2.1 Internal Memory Architecture

4.2.1.1 Configurable Memory Blocks (Cache/SRAM)

4.2.2 Instruction Memory and Control Registers

4.2.3 Data Memory and Control Registers

4.3 Cache Operation

4.3.1 Instruction Cache Mode

4.3.2 Data Cache Mode

4.3.3 Cache control Instructions

4.4 Memory Protection

4.4.1 CPLBs (Cachability Protection Lookaside Buffers)



5 Program Sequencer

5.1 Features

5.2 Conditional Sequencing

5.3 Instruction Pipe Line

5.3.1 Synchronizing pipeline to Core/System events

5.3.2 Stalls and avoiding them

5.3.3 Pipeline viewer

5.4 Branching

5.4.1 Conditional vs Unconditional

5.4.2 Zero Overhead Looping

5.4.3 Compiler branch/loop optimizations

5.5 Event Controller

5.5.1 Interrupt vs Exception Handling

5.5.2 CEC (Core Event Controller) and SIC (System Interrupt Controller)

5.5.3 Interrupt processing flow

5.5.4 Interrupt handling in C

5.5.5 System Services support for Interrupt Handling

6 Linker Operations

6.1 Converting C and Assembly files to Object files

6.1.1 Features and Overview

6.1.2 Assembler Expressions and Directives

6.1.3 Object Sections

6.1.4 Definition Files

6.2 Linker / Linker Description File (LDF)

6.2.1 Features and Overview

6.2.2 LDF Commands

6.2.3 Example LDF

6.2.4 Linker Optimizations

6.2.5 Expert Linker

6.2.6 The Linker and the C Run Time Environment

6.3 Project Wizard customization of the System Memory usage



-
- 7 Advanced Instructions**
 - 7.1 8-bit ALU Instructions**
 - 7.1.1.1 Compiler builtin support for Video ALU**
 - 7.2 Vector Operations**
 - 7.3 Issuing Parallel Instructions**
 - 7.4 Other Code Optimization Topics**

 - 8 Timers and Flags**
 - 8.1 Timer Overview**
 - 8.1.1 Timer API under System services**
 - 8.2 Core Clock**
 - 8.3 Real Time Clock**
 - 8.4 Watch Dog Timer**
 - 8.5 GP Timers**
 - 8.5.1 PWM Mode**
 - 8.5.2 Pulse Capture Mode**
 - 8.5.3 External Clock Mode**
 - 8.6 Programmable Flags Overview**
 - 8.6.1 Multiplexing with peripheral functions**
 - 8.7 ADSP-BF537 IO Ports**
 - 8.7.1 Configuration**
 - 8.7.2 Port support under System Services**



9 Direct Memory Access (DMA)

9.1 Overview

9.2 DMA channel priorities

9.3 DMA Mapping with SSL

9.4 Setting up DMAs

9.4.1 Register based DMA

9.4.2 Descriptor based DMA

9.4.3 SSL Data Structures

9.5 Peripheral ↔ Memory transfers

9.5.1 Opening a Peripheral DMA Channel with SSL

9.6 Memory ↔ Memory transfers

9.6.1 Opening a Memory DMA Channel with SSL

9.7 DMA Traffic control

9.8 2D DMA

10 External Bus Interface Unit (EBIU)

10.1 Features and Overview

10.2 External Memory Interface

10.2.1 Asynch Memory Controller

10.2.2 SDRAM Controller

10.3 Performance

11 Serial Communications

11.1 Serial Port (SPORT)

11.1.1 Features

11.1.2 Pin Descriptions

11.1.3 Modes of Operation

11.1.4 Configuration

11.2 Serial Peripheral Interface (SPI)

11.2.1 Features and Setup

11.3 UART

11.3.1 Features and Setup



12 PPI

- 12.1 What is PPI?**
- 12.2 Operating Modes**
- 12.3 Video Basics**

13 System Booting

- 13.1 Booting Modes**
- 13.2 Loader file formats**
- 13.3 Multi Application Booting**
- 13.4 VisualDSP Loader Utility**

14 System Design

- 14.1 Operating modes**
- 14.2 Dynamic Power Management**
 - 14.2.1 Clock generation / PLL**
 - 14.2.2 Power-down modes**
- 14.3 Resetting the DSP**
- 14.4 JTAG Overview**
- 14.5 Board Design and Layout**
- 14.6 Debug Registers**

15 Optimization Topics

- 15.1 Overview**
- 15.2 General Approach to Optimization**
- 15.3 Algorithmic considerations**
- 15.4 Getting to know the Compiler**
 - 15.4.1 Optimization Switches and pragma's**
 - 15.4.2 Built-in functions**
 - 15.4.3 Example compiler output**
 - 15.4.4 PGO (Profile Guided Optimization)**
 - 15.4.5 C++ considerations**
 - 15.4.6 Summary**



-
- 15.5 Where to start optimizing?
 - 15.5.1 Using the profiler effectively
 - 15.6 Assembly Language Interfacing
 - 15.6.1 CRT Stack
 - 15.6.2 Parameter passing
 - 15.6.3 Register usage
 - 15.6.4 C-Callable assembly function example
 - 15.6.5 Inline assembly
 - 15.7 Video Frameworks
 - 15.7.1 Challenges
 - 15.7.2 Common Frameworks

 - 16 Using System Services and Device Drivers
 - 16.1 Project considerations when using Device Drivers
 - 16.1.1 Memory requirements
 - 16.1.2 Interpreting Result Codes
 - 16.2 Detailed example walkthrough
 - 16.2.1 Initialization of the various services
 - 16.2.2 Customization considerations for custom hardware
 - 16.2.3 Setting up deferred callbacks
 - 16.2.4 Opening a device driver and peripheral setup
 - 16.2.5 Structure of the callback function
 - 16.3 Exercise

 - 17 Hardware Tools
 - 17.1 Overview with Part Numbers
 - 17.2 ADSP-BF533 EZ-Kit
 - 17.3 ADSP-BF537 EZ-Kit
 - 17.4 EZKIT Extender Boards
 - 17.5 In Circuit Emulators (ICE)

 - 18 Two Wire Interface (TWI)
 - 18.1 What is it?
 - 18.2 Master mode example
 - 18.3 Slave mode example



19 CAN Interface

- 19.1 Controller Area Network Overview**
- 19.2 Data Link Layer**
 - 19.2.1 CAN message format**
 - 19.2.2 Bus Arbitration**
 - 19.2.3 CAN Implementation on the Blackfin® Processor**
 - 19.2.4 Setting up Mailboxes**
 - 19.2.5 Sending/Receiving messages**
 - 19.2.6 Additional Blackfin® processor features**
- 19.3 Software**
 - 19.3.1 Examples**
 - 19.3.2 3rd party drivers**

20 Ethernet MAC

- 20.1 Overview**
- 20.2 Lower levels**
 - 20.2.1 Blackfin® Ethernet MAC Features and Overview**
 - 20.2.2 System interface considerations**
 - 20.2.3 Drivers**
- 20.3 Higher levels**
 - 20.3.1 TCP/IP Stack options**
 - 20.3.2 Developing applications with lwIP protocol stack**
 - 20.3.2.1 Configuring lwIP**
 - 20.3.2.2 Example application**

21 VDK Introduction

- 21.1 Threads and scheduling**
- 21.2 VDK projects**
- 21.3 Signaling and synchronization**
- 21.4 I/O devices and drivers**
- 21.5 Memory pools and messaging**
- 21.6 Multiple heaps**
- 21.7 VDK Conventions**
- 21.8 Error handling**
- 21.9 Debug assistance**