Course Name:	System Development and Programming with the ADSP-TS101 (TigerSHARC)
Course Number:	ADST-160
Course Description:	This is a practical course with 'hands on' training using the latest VisualDSP++ software development tools. First the core elements of the processor, which includes the Computational Units, the Integer ALUs, and the Program Sequencer, are examined in detail along with the relevant assembly code instructions. A number of simulator labs help in understanding operation of the individual elements. Memory configuration (both internal and external) is discussed next. Advanced instructions are presented with a follow on lab on code optimization. The I/O peripherals, which include the Link Ports and External Port, are discussed in detail along with DMA operation between these peripherals and internal memory. This section also deals with system booting and other features including timers and SDRAM controller. Finally, hardware development tools, such as evaluation boards and ICE's are introduced. Throughout the course, the various aspects of the software development process using the latest tools are discussed including setting up and building projects, assembly language programming, code debugging, simulation, tool support for code overlays and shared memory, and 'C' programming support.
Goals/Objectives:	The main course objective is to understand the architecture of the ADSP-TS101 DSP sufficiently to enable DSP system designers to resolve hardware/software issues with their applications. Additional goals include gaining a thorough understanding of both assembly language programming and code development (including 'C' programming issues) with the latest software tools
Pre-requisites:	Previous embedded microprocessor background would be an asset (hardware and/or software)
Target Audience:	System Designers needing to make informed decisions on design tradeoffs, Hardware Designers needing to develop external interfaces, and Code Developers needing to know how to get the highest performance from their algorithms
Target Duration:	3.5 days

11 Advanced Instruction Types

11.1 Communications Instructions

11.2 Reciprocal and Divide

11.3 Reciprocal Square Root and Square Root

12 Code Optimization

12.1 Parallel Instruction Types and Multifunction Computations

12.2 Optimization techniques

12.3 Simulator Exercise*:* code optimization

13 I/O Processor

13.1 IOP Structure

13.1.1 I/O Processor Features

13.2 DMA Unit

13.2.1 DMA Architecture

13.2.2 DMA Features

13.2.3 DMA modes & examples

13.2.4 External Port DMA

13.3 External Port

13.3.1 Memory Interface

13.3.2 Shared Bus Multiprocessing (Cluster mode)

13.3.3 Host Interface

13.4 SDRAM interface

13.5 Link Port

13.5.1 Link Port Features

13.5.2 Link Port Configuration—DMA & Control

13.5.3 Link Port Pin Description & Function

13.6 Timers